Max-Planck-Institut
für Radioastronomie

CSO-FFTS

A Fast Fourier Transform Spectrometer for the CSO

Design Description

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1 Purpose

The purpose of this document is to provide an overview on the technical data for the CSO-Fast Fourier Transform Spectrometer (CSO-FFTS).

2 Reference Documents

RD-01	CSO-Fast Fourier Transform Spectrometer, Design Description, CSO-MPI-DSD-02
RD-02	CSO-Fast Fourier Transform Spectrometer, User Manual, CSO-MPI-MAN-02
RD-03	APEX SCPI socket command syntax and backend data stream, APEX-MPI-IFD-0005
RD-04	B. Klein, S.D. Philipp, I. Krämer et al., 2006, A&A, 454, L29
RD-05	B. Klein, S.D. Philipp, R. Güsten et al., 2006, SPIE Vol. 6275, pp. 627511
RD-06	D. Muders, H. Hafok, F. Wyrowski et al., 2006, A&A, 454, L25
RD-07	Acqiris documentation, available at www.acqiris.com

3 Definitions

Within this document we will use the following abbreviations:

IF	CSO Heterodyne IF system, delivered by MPIfR
FFTS	Fast Fourier Transform Spectrometer, user manual
ADC	Analog-to-Digital Converter
FPGA	Field Programmable Gate Array
MPIfR	Max-Planck-Institut für Radioastronomie

4 Introduction / Technical Specifications

The Fast Fourier Transform Spectrometer for the CSO (CSO-FFTS hereafter) is a novel high-resolution 1 GHz spectrometer, which technology has been proven to be capable of operating at high altitudes (e.g. APEX, 5100-m) (see RD-04 & RD-05).
The technical specifications and performance parameter for the CSO FFTS are equal to the well tested APEX FFT spectrometers, which are in successful operation since April 2005 (RD-04).
The CSO FFTS is based on the currently most powerful digitizer/analyzer board (AC240, Fig. 1) available from Acqiris, Switzerland. It incorporates two 1 GS/s ADCs which feed a XILINX VirtexII Pro70 FPGA chip (Fig. 2; for technical details see table section 4.1). By combining both ADCs in an interleave manner (180 deg phase-shift), the AC240 is capable of sampling an analog input signal at 2 GHz clock rate which results in a 1 GHz Nyquist bandwidth. The accurate interleave adjustment (calibration) of both ADCs is realized by a control circuit and an on-board clock generator. The sample rate for both ADCs is selectable by software in a 1, 2, 2.5, 4 and 5 sequence, resulting in 100 MS/s to 2 GS/s. For multi-board applications which need a synchronized sampling, the time base of the clock generator can be driven from an external reference frequency. The AC240's 50 signal inputs feature programmable frontend electronics with input voltage ranges selectable in 7 steps from 50mV to 5V and variable voltage offsets. The board allows both AC and DC input signal coupling. In addition, a programmable trigger-input enables an external start of sampling and data processing. The AC240 is designed as a standard 6U compact PCI/PXI board. Processed digitized data can be transferred, in direct memory access-mode (DMA), directly to the host PC via the PCIbus at sustained rates of up to 100 MB/s. For a more detailed description of the AC240 Board, we refer to the Acqiris documentations (RD-07).

Fig. 1: Photo of the AC240 digitizer board. The AC240 is a dual-channel 6U compact PCI/XI digitizer with an onboard real time processing unit. The picture shows on the top the two analog inputs for the signal at intermediate frequency (DC-1 GHz), an input for trigger and/or clock, and the system control interface. The FPGA processing unit is visible on the right side, and the PCI bus for data output is shown at the bottom left (www.acqiris.com).

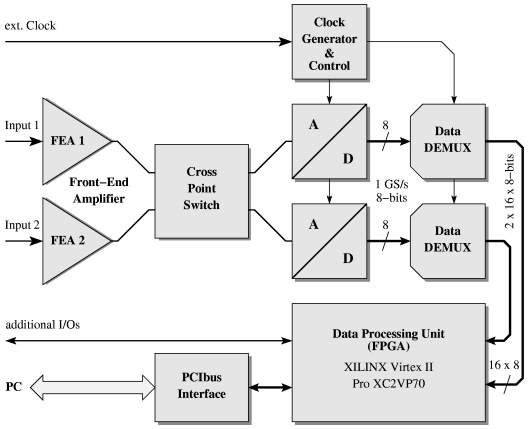

Fig. 2: Block diagram of Acqiris' AC240 digitizer/ analyzer board, the main hardware of the FFT spectrometer. By applying interleaved techniques, the two 1 GS/s 8-bits ADCs can be combined to one 2 GS/s converter. To feed the high data rate output of the ADCs (2 GBytes/s) to the FPGA, de-multiplexers (DEMUX) are used which split the two 8-bits data streams at 1 GHz to 2x16 streams at 62.5 MHz, suitable for the FPGA.

4.1 Hardware specifications of the ADC/FPGA boards (Acqiris, AC240)

ADC input sampling rate	2 Giga samples / sec
ADC input bandwidth (-3 dB)	0 – 1 GHz
ADC input resolution (quantization)	8 Bit
Input full scale range	50 mV – 5 V (-22 dBm – 16 dBm @50Ω)
Input coupling	AC (default) / DC
Maximum dynamic range	48 dB
Ghost free dynamic range	> 30 dBm
SFDR (spurious-free dynamic range)	37 dB
FPGA Data Processing Unit	XILINX Virtex 2 PRO 70
Compact PCIbus interface	32-Bit / 33 MHz
Operating temperature	0°…30°
Relative humidity (non condensing)	5…90%

4.2 Specifications of the IRIG-B/Blank-Sync board

The IRIG-B/Blank-Sync board serves two purposes. On the one hand it provides the time-stamping of the data stream, on the other hand it is used for the synchronization of the FFTS with the timing signal from the telescope control system. This card, together with the AC240 board, is integrated into a dedicated FFTS PC. The layout of the board including the pin allocation is shown in Figs. 3 – 5.

Fig 3: Photo of the IRIG-B board, as developed in the DigitalLabor of the MPIfR

Pin	**Signal**
1	SYNC -
9	SYNC +
2	BLANK -
10	BLANK +
3	S0 -
11	S0 +
4	S1 -
12	S1 +
5	S2 -
13	S2 +
6	STROBE -
14	STROBE +
7	no connection
15	GND

Table 1: IRIG-B board: Pin assignment of the 15 pin Sub-D connector

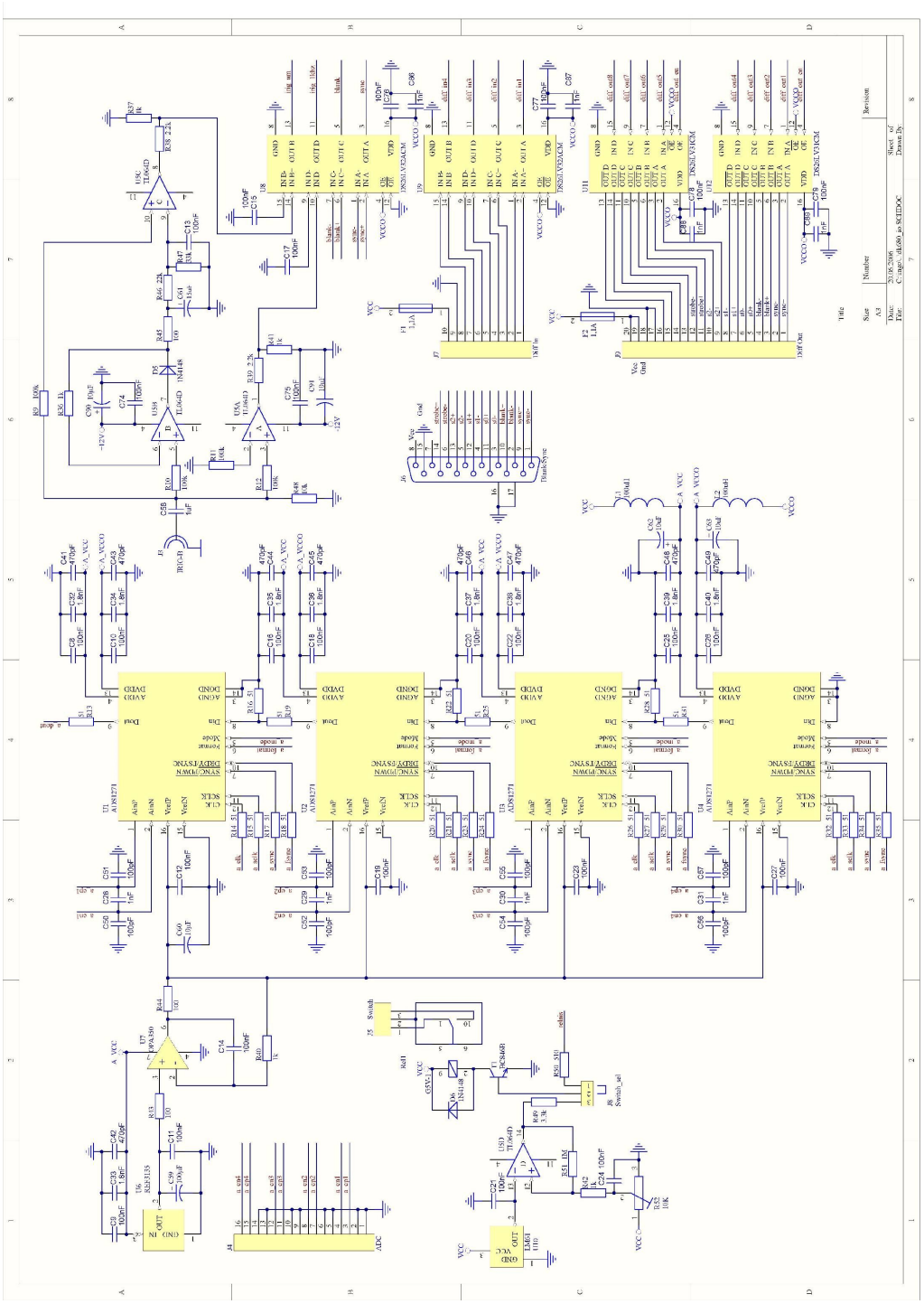

Fig 4: Circuit diagram of the IRIG-B board part1

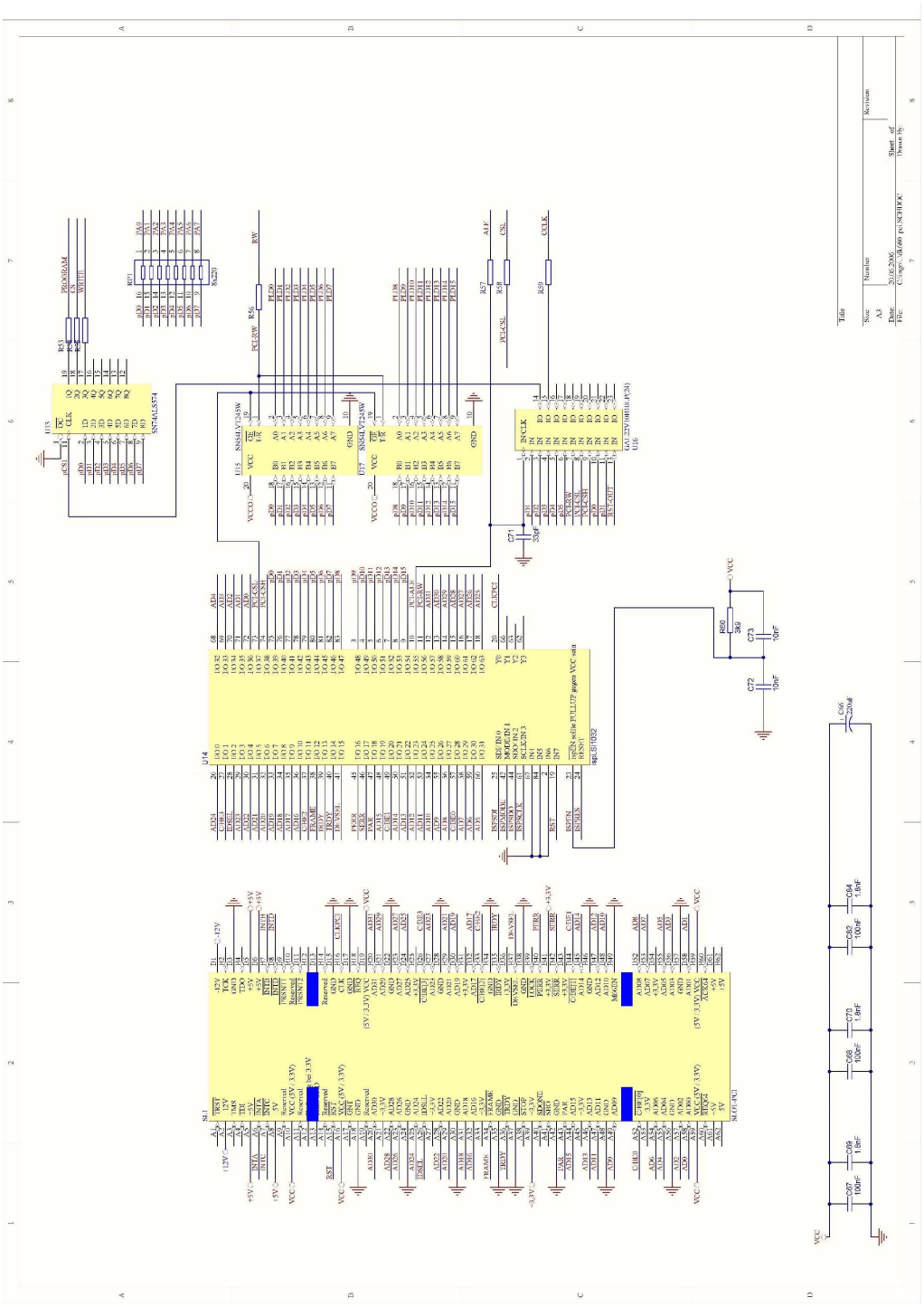

Fig 5: Circuit diagram of the IRIG-B board part 2

5 FPGA/FFT process pipeline

The spectrometer core development was contracted to RF Engines Ltd. (RFEL), following our guidelines, and was finally integrated at MPIfR digital group. The spectrometer core is based on RFEL's HyperSpeed Fast Fourier Transform (FFT) technology (technical details are listed in the table section 5.1). It receives 8-bit samples from the two ADCs at a continuous sample rate of 2 GHz, and then processes this data in a sequence of four steps:

- ◊ First a Half Band Filter converts samples to a complex I/Q-format, and reduces the sample rate by a factor of two (decimation by two), which eases the subsequent processing requirements.
- ◊ This is followed by the application of a windowing function (Blackman-Harris), which weights the data in order to control the filtering performance of the FFT. The window coefficients are user programmable at run-time, allowing the performance characteristics of the spectrometer to be modified for changing operational scenarios.
- ◊ The 32K-point HyperSpeed FFT core from RFEL forms the central element of the system, performing the conversion from the time-domain to the frequency-domain, and it includes bit reversing to sort the data in natural frequency order. The FFT is built using a highly parallel architecture in order to achieve the very high data rate of 2 Gbytes/sec.
- ◊ The final step of processing contains the conversion of the frequency spectrum to a power representation, and successive accumulation of these results. This accumulation step has the effect of averaging together a number of power spectra, thereby reducing the background noise and improving the detection of weak signals. This step also reduces the huge amount of data produced by the prior stages, and eases any subsequent interface bandwidth requirements and processing loads. The output from the spectrometer core is in a 32-bit floating-point format, which allows data to be efficiently post-processed by standard desktop computers. The processing sequence is shown below.

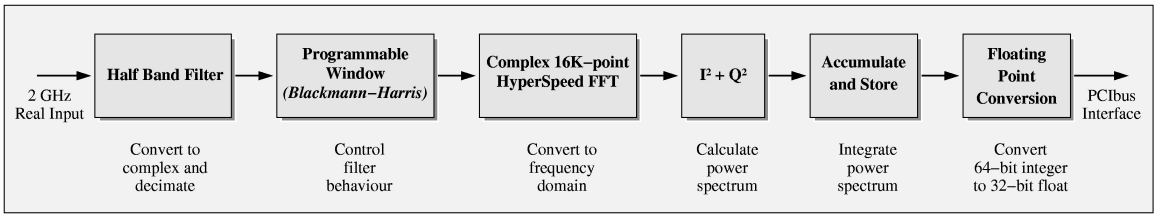

Fig. 6: Real-time FFT processing pipeline

5.1 Frequency resolution of the FFTS

To understand the spectral resolution and effective channel bandwidth of the FFTS, the spectral leakage caused by the application of the Fourier Transform (FFT) to a noisy signal must be considered. Spectral leakage is the result of the assumption in the FFT algorithm that the signals are contained in a single FFT time record and thus periodic at intervals corresponding to the length of this time record. If the time record has a non-integral number of cycles, this assumption is violated and spectral leakage occurs, which introduces a wide range of frequencies in the frequency domain and results in the energy of a signal spreading to adjacent frequency bins. If no window function is applied prior to the FFT, the first sidelobes are attenuated by 13 dB relative to the main-lobe and the sidelobe fall-off rate is 6 dB per octave. Consequently, the selectivity of a bare FFT is poor, which results in a large amount of ripples in the passband. In addition, the spectral leakage from a large signal component may be so severe that other weaker signals at different frequencies are masked. The effects of spectral leakage can be restricted by reducing the discontinuities at both ends of the time record, i.e. by multiplying the data

with a suitable window function. For radio astronomical applications a Blackman-Harris window is adequate due to its excellent spectral leakage attenuation and good amplitude conservation for random and noisy input signals. The APEX FFTS applies a 3-term Blackman-Harris window. Unfortunately, there is always a trade-off between the main-lobe width and the sidelobe leakage: As the sidelobe level decreases, the main-lobe width is increased. To characterize this behavior the equivalent noise bandwidth (ENBW) is usually used. The ENBW indicates the equivalent rectangular bandwidth of a filter with the same peak gain that would result in the same output noise power. Table 1 is a comparison of the properties of a rectangular, a Hanning and a Blackman-Harris window. Since the ENBW for a rectangle filter is 1.0, which is equal to the channel separation frequency (61.035 kHz), the frequency resolution for the CSO FFTS, applying the Blackman-Harris window, is 98.267 kHz.

5.2 Specification of the FPGA/FFT-processing pipeline

Fast Fourier Transform (FFT)	RFEL, HyperspeedFFT
FFT:: Number of frequency channels	16484
FFT:: Frequency channel separation	61.035 kHz
FFT:: Frequency resolution (Blackman-Harris-Window)	98.267 kHz
FFT:: Adjacent channel rejection - no binning (16384 channels) - binning 2 (8192 channels)	 > 15 dB ~ 48 dB
FFT:: Arithmetic	2's complement, 18-bit
Digital Half Band Filter (DHBF)	50 - 950 MHz
DHBF:: Stopband rejection	-48 dBm
DHBF:: Passband ripple	+/- 0.1 dB (max.)
Power Spectra Builder (sum of squares)	Full precision, 33-Bit
On-board accumulation (integration)	54-bit precision
On-board accumulation:: min time	32.768 µs
On-board accumulation:: max time (full precision)	~ 35 seconds
Fastest spectral dump-time	< 100 ms
Stability / Allan-Variance time in the lab	~ 4000 sec (see Fig. 7)

N.B.: With the current IF-unit the usable bandwidth is limited to ~950MHz to avoid aliasing effects at the band edges.

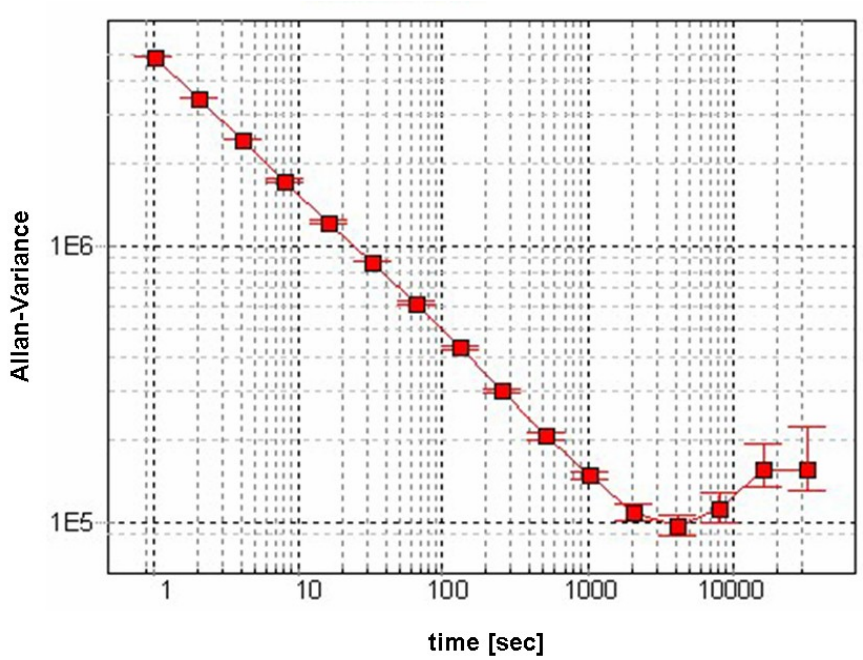

Fig.7: The excellent stability of the FFTS is illustrated in this Allan-Variance-Plot. The signal of a noise source (0–1 GHz) was integrated and processed in the FFTS. The spectroscopic variance between two 1 MHz broad channels, separated by 600 MHz within the band, was determined to be stable on a timescale of ~4000 s.

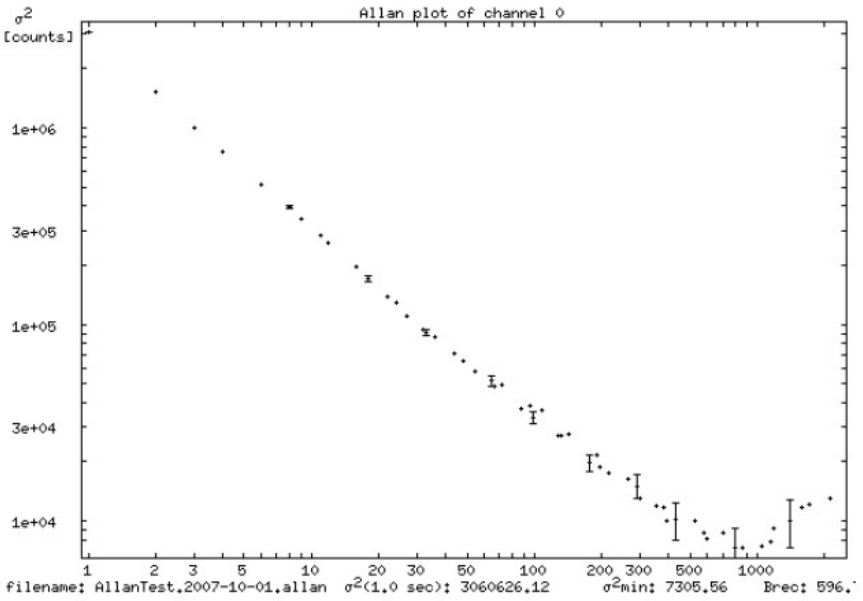

Fig.8: Spectroscopic Allan stability of the CSO-FFTS connected with the CSO-IF processor. Similar to fig.7, the variance is calculated for two 1 MHz broad channels which are separated by 600 MHz within the 1 GHz band.

6 FFTS-Interfaces

6.1 CSO-FFTS: SCPI command interface

The FFTS is controlled by the SCPI command interface, which is structured along the baselines documented in RD-06.

The following tables show the actually implemented CORBA commands.

CSO:FFTS1 CORBA Object

Methods:

Name	*Comments*
on	switch FPGA/FFT processing pipeline on
off	switch FPGA/FFT processing pipeline to power save
reset	- not implemented -
configure	FFTS must be *stopped* before sending this command
start	starts measurement with first phase
stop	stops measurement after last phase
abort	stops measurement after actual phase
extRefFreq	use external reference frequency (10 MHz)
intRefFreq	use internal reference frequency (10 MHz)

Properties:

Name	*Defaults*) / Parameter range*	*Comments*
state	ENABLED or DISABLED or SHUTDOWN	
integrationTime	actual measured integration time integrationTime ≤ MIN{ (SYNC-BLANK, cmdIntegrationTime) }	If FFTS is *stopped: intTime = 0 ms*
cmdIntegrationTime	default: 8000 ms	mind. 100 ms
usedSections	default: sections = 0	
cmdUsedSections	default: sections = 0	
blankTime	default, INTERNAL mode: 5.000 µs	BLANK < SYNC
cmdBlankTime	default, INTERNAL mode: 5.000 µs	mind. 5.000 µs

Name	*Defaults*) / Parameter range*	*Comments*
syncTime	default, INTERNAL mode: 500.000 µs	
cmdSyncTime	default, INTERNAL mode: 500.000 µs	100 ms ≤ Sync ≤ 5 s
numPhases	default, INTERNAL mode: 2	
cmdNumPhases	default, INTERNAL mode: 2	Phases: 1 .. 4
mode	INTERNAL / EXTERNAL	
cmdMode	default: INTERNAL	
version	1.16 (1 GHz / 16K channels)	
release	(e.g. Nov_28_2007)	
temperature	Temperature = MAX(board1.temp, board2.temp)	FPGA temperature in °C

*) after re-start / reboot!

CSO:FFTS1:BAND1 CORBA Objects:

Properties:

Name	*Defaults*) / Parameter range*	*Comments*
numSpecChan	default: 16'384	
cmdNumSpecChan	default: 16'384 range: 1 – 16'384 in power 2 steps	
bandWidth	default: 1 GHz	fixed!
cmdBandWidth	default: 1 GHz	fixed!
chanWidth	30,5 kHz – 1 GHz	
IFAtten	default: +10 dBm (2 Vpp @ 50 Ohm)	
cmdIFAtten	default: +10 dBm (2 Vpp @ 50 Ohm) -22, -16, -10, -2, +4, +10, +18 dBm	
IFLevel	estimated IF level (from spectra)	
minIFLevel	min. IF level in selected range	
maxIFLevel	max. IF level in selected range	
temperature	temperature of selected band	FPGA temperature, °C

6.2 CSO-FFTS: SCPI data stream interface

The FFTS uses a TCP-network connection to transmit the spectral data to the observing system (e.g. the FitsWriter). The implemented protocol is compatible to the SCPI backend data stream interface, which is structured along the baselines documented in RD-06.

7 Technical environment data of the CSO-FFTS

Total weight	FFTS and FFTS-PC: appr.: 35kg
Volume of the unit	FFTS: ~2 height units 19” FFTS-PC: 3 height units 19” Keyboard: ~1 height unit 19” TFT-display: 9 height units 19”
Power consumption (FFTS and FFTS-PC)	< 300W, 110V/60Hz
Network connection	RJ45, 100 MBit/s Ethernet
Time synchronisation	IRIG-B (AM) time signal
Measurement synchronisation	BLANK-/SYNC-signal, differential

The FFTS is protected against overheating by software:
The FPGA chip is switched to idle-mode in case the temperature of the FPGA rises above 65°C. As soon as the temperature decreases below that level the FFTS can be operated again.

8 LabView Interface

There is an online display and interface available for the CSO-FFTS, which is implemented as a LabView application. A more detailed description of this interface and its functions will be provided in a dedicated user manual (RD-02).

Fig.9: Display of the LabView-GUI. In the upper panel the bandpass of the FFTS spectrum is shown, in the lower panel difference of two sequencing dumps is plotted. On the right side the operational parameters and settings are listed.