TIP605

16 Digital Inputs
Optically Isolated
Version 1.0 Revision A

User Manual

Issue 1.0

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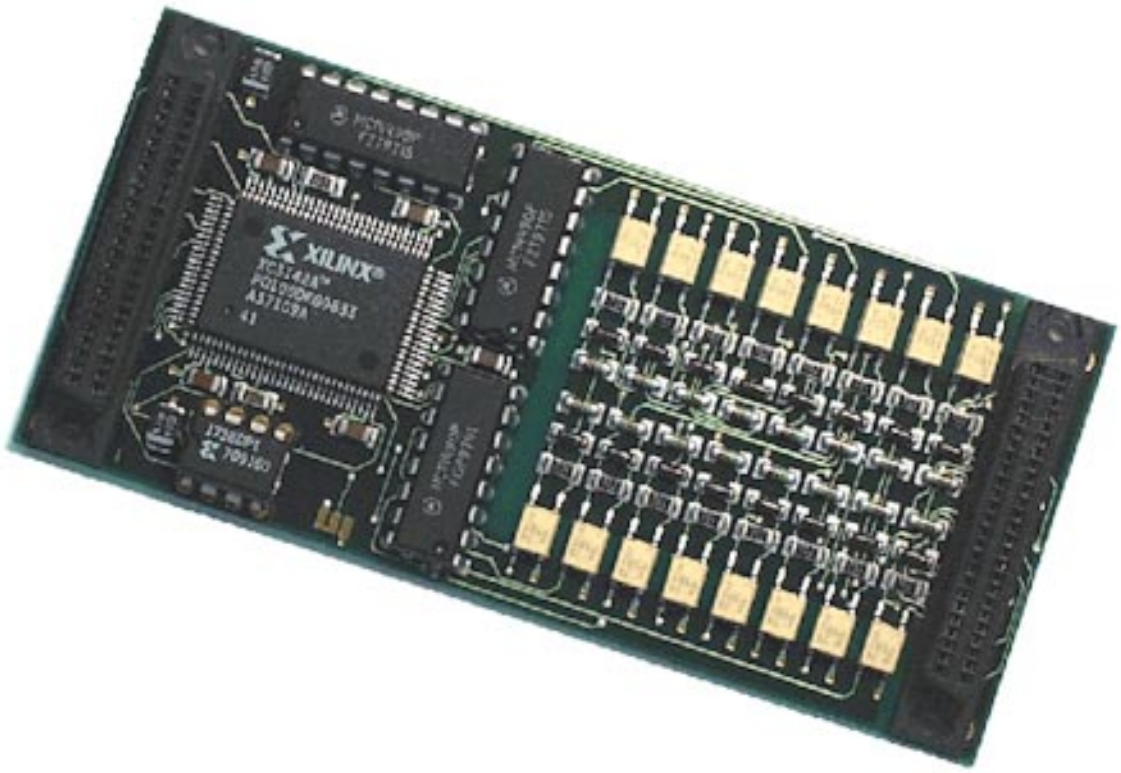


TIP605-10
16 Digital Inputs
Optically Isolated

Issue	Description	Date
1.0	Prel. Version	12 May 1997

1. Product Description

The TIP605 is an IndustryPack® compatible I/O module with digital inputs interfacing directly to 24 volt DC control voltage. Each of the 16 inputs may generate interrupts.

The16 digital inputs are galvanically isolated by optocoupler. The individual inputs are potential free in relation to each other. All inputs have an electronic debounce circuit. The debounce time is programmable in a range from 8µs up to 261ms in steps of 1,024 ms. (default debounce time is 8µs)

All inputs can generate interrupts . The signal edge handling to generate interrupts is programmable. By this it is possible to choose between rising and falling or both edges.

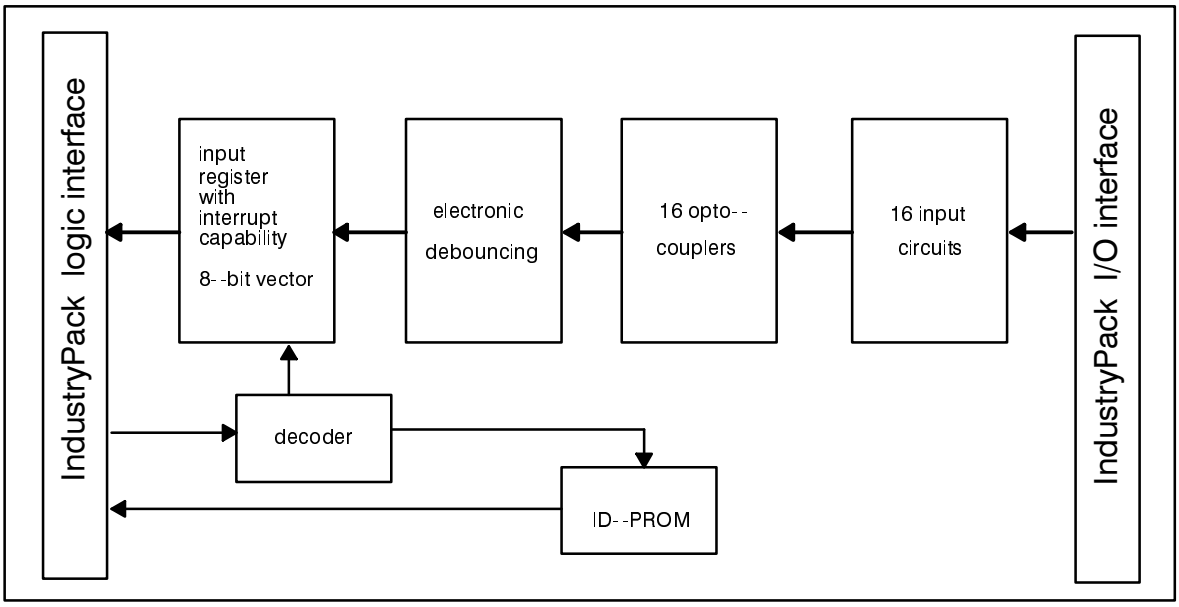


Figure 1: TIP605 Block Diagram

2. Technical Specification

Logic Interface	IndustryPack® Logic Interface
Size	single-size IP
I/O Interface	50-conductor flat cable
Number of Inputs	16, each input can generate an interrupt at programmable signal transition
Input Isolation	All channels, completely independent from each other
Input Voltage	24V DC
Input Current	4.2 mA at 24V input voltage
Input Switching Level	12V (minimum 7.5V, maximum 14V)
Input Signal Debouncing	Electronic debouncing with programmable debounce time (8 µs to 261 ms in 1,024 ms steps common for all inputs)
Wait States	$\overline{\text{IOSEL}}$: no wait states $\overline{\text{INTSEL}}$: no wait states $\overline{\text{IDSEL}}$: no wait states
Power Requirements	tbd
Temperature Range	Operating -40°C to 85°C Storage -55°C to 125°C
Humidity	5 - 95% non-condensing

3. ID Prom Contents

ADDRESS	FUNCTION	CONTENTS
$ 01	ASCII 'I'	$ 49
$ 03	ASCII 'P'	$ 50
$ 05	ASCII 'A'	$ 41
$ 07	ASCII 'C'	$ 43
$ 09	Manufacturer ID	$ B3
$ 0B	Model Number	$ 1A
$ 0D	Revision	$ 10
$ 0F	RESERVED	$ 00
$ 11	Driver-ID low-byte	$ 00
$ 13	Driver-ID high-byte	$ 00
$ 15	number of bytes used	$ 0D
$ 17	C R C	$ 1F
$ 19	Version -10	$ 0A

Figure 2: ID PROM Contents

4. TIP605 Addressing

The TIP605 is accessed in the I/O space through a set of registers.
Address range: ip_io_base_address + ($00 to $0F)

ADDRESS	NAME	FUNCTION	SIZE
$ 00	DATAREG	Input Data Register	word
$ 03	INTCONT	Global Interrupt Control Register	byte
$ 04	INTENALH	Interrupt Enable Rising Edge	word
$ 06	INTENAHL	Interrupt Enable Falling Edge	word
$ 08	INTSTATLH	Interrupt Status Rising Edge	word
$ 0A	INTSTATHL	Interrupt Status Falling Edge	word
$ 0D	INTVEC	Interrupt Vector Register	byte
$ 0F	DEBTIME	Debounce Time Register	byte

Figure 3: TIP605 Register Map

Note

All registers are set to zero after reset.

4.1. Input Data Register

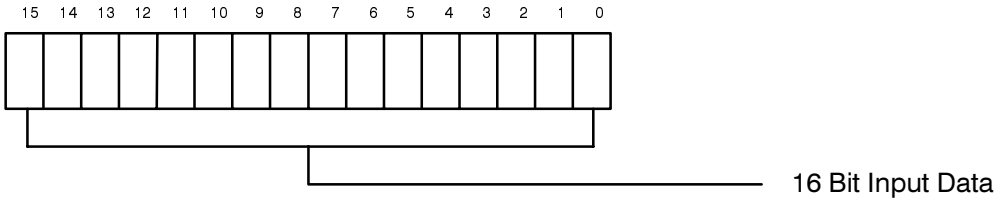


Figure 4: Input Data Register

The Input Data Register is a read only register that reflects the actual states of the inputs.

4.2. Global Interrupt Control Register

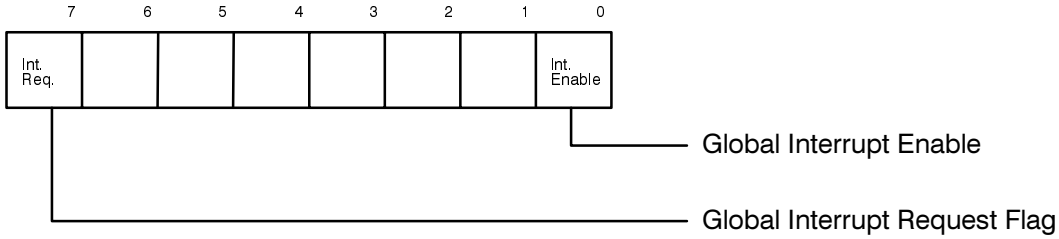


Figure 5: Global Interrupt Control Register

Bit 0 of the Global Interrupt Control Register is used as a global interrupt enable. This bit is a read/write bit. Writing a '1' to bit 0 of the Global Interrupt Control Register globally enables interrupts for all 16 inputs on interrupt request line $\overline{\text{INTREQ0}}$ of the IP bus.
Bit 7 of the Global Interrupt Control Register reflects the state of the Global Interrupt Request Flag . This bit is a read only bit. If this bit is read as '1', than an interrupt request of at least one of the 16 input channels is pending.

Bit 1 to 6 of the Global Interrupt Control Register are not used and undefined during reads.

4.3. Interrupt Enable Register Rising Edge

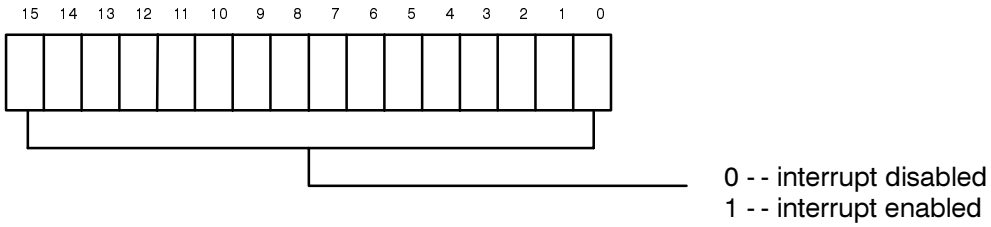


Figure 6: Interrupt Enable Register Rising Edge

The Interrupt Enable Register Rising Edge is a word wide read/write register. Bit 0 of the Interrupt Enable Register Rising Edge enables interrupts of input channel 1 for the rising edge. Bit 15 enables interrupt of input channel 16 for the rising edge.

Note

An interrupt request on interrupt request line $\overline{\text{INTREQ0}}$ of the IP bus is only generated if the Global Interrupt Enable bit of the Global Interrupt Control Register is set to '1'.

4.4. Interrupt Enable Register Falling Edge

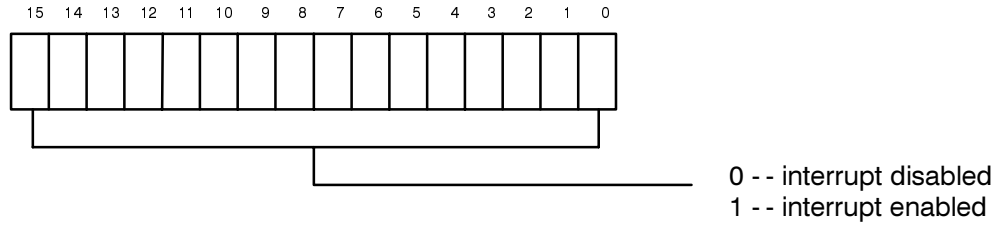


Figure 7: Interrupt Enable Register Falling Edge

The Interrupt Enable Register Falling Edge is a word wide read/write register. Bit 0 of the Interrupt Enable Register Falling Edge enables interrupts of input channel 1 for the falling edge. Bit 15 enables interrupts of input channel 16 for the falling edge.

Note

An interrupt request on interrupt request line $\overline{\text{INTREQ0}}$ of the IP bus is only generated if the Global Interrupt Enable bit of the Global Interrupt Control Register is set to '1'.

4.5. Interrupt Status Register Rising Edge

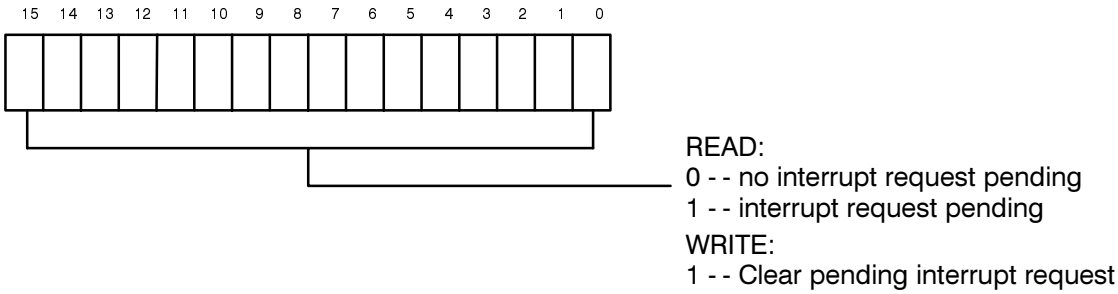
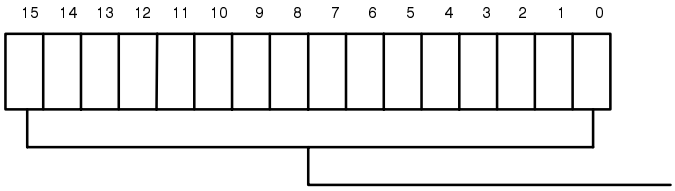


Figure 8: Interrupt Status Register Rising Edge

The Interrupt Status Register Rising Edge is a word wide read /write register. Bit 0 of this register reflects the interrupt request state of input 1 for the rising edge, bit 15 of this register reflects the interrupt request state of input 16 for the rising edge. An interrupt request for a specific input is cleared by writing a '1' to the according bit of the Interrupt Status Register Rising Edge.

4.6. Interrupt Status Register Falling Edge

Figure 9: Interrupt Status Register Falling Edge



READ:
0 - - no interrupt request pending
1 - - interrupt request pending
WRITE:
1 - - Clear pending interrupt request

The Interrupt Status Register Falling Edge is a word wide read /write register. Bit 0 of this register reflects the interrupt request state of input 1 for the falling edge, bit 15 of this register reflects the interrupt request state of input 16 for the falling edge.
An interrupt request for a specific input is cleared by writing a '1' to the according bit of the Interrupt Status Register Falling Edge.

4.7. Interrupt Vector Register

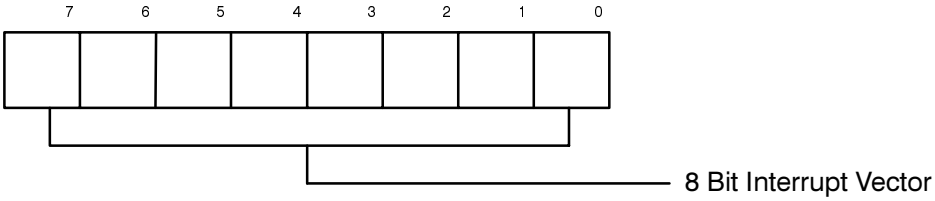


Figure 10: Interrupt Vector Register

The Interrupt Vector Register is a byte wide read/write register. The 8 Bit interrupt vector is loaded by software.

4.8. Debounce Time Register

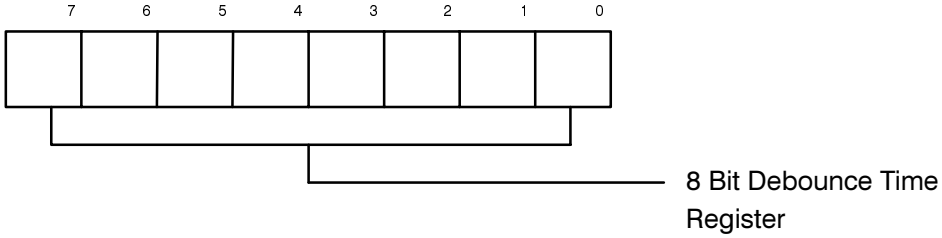


Figure 11: Debounce Time Register

The Debounce Time Register is a byte wide read/write register. The value 0 in this register sets the debounce time to a minimum of 8µs (default after reset).
The debounce time can be programmed in steps of 1.024 ms in the range of 8 µs to 261 ms. The debounce time is common for all inputs.

$$\text{Preload value} = \frac{\text{Debounce Time (ms)}}{\text{1,024 (ms)}}$$

5. Installation

5.1. Input Wiring

Each input is optically isolated from the logic circuit. Each input is independent of the other inputs and can be wired different. Each input has two connections at the IP I/O connector, Input x + and Input x -. All inputs are isolated by optocoupler and against each other. The inputs channels can be activated only in one polarity and have an external diode to prevent damage of the optical coupler by wiring the input in a wrong direction.

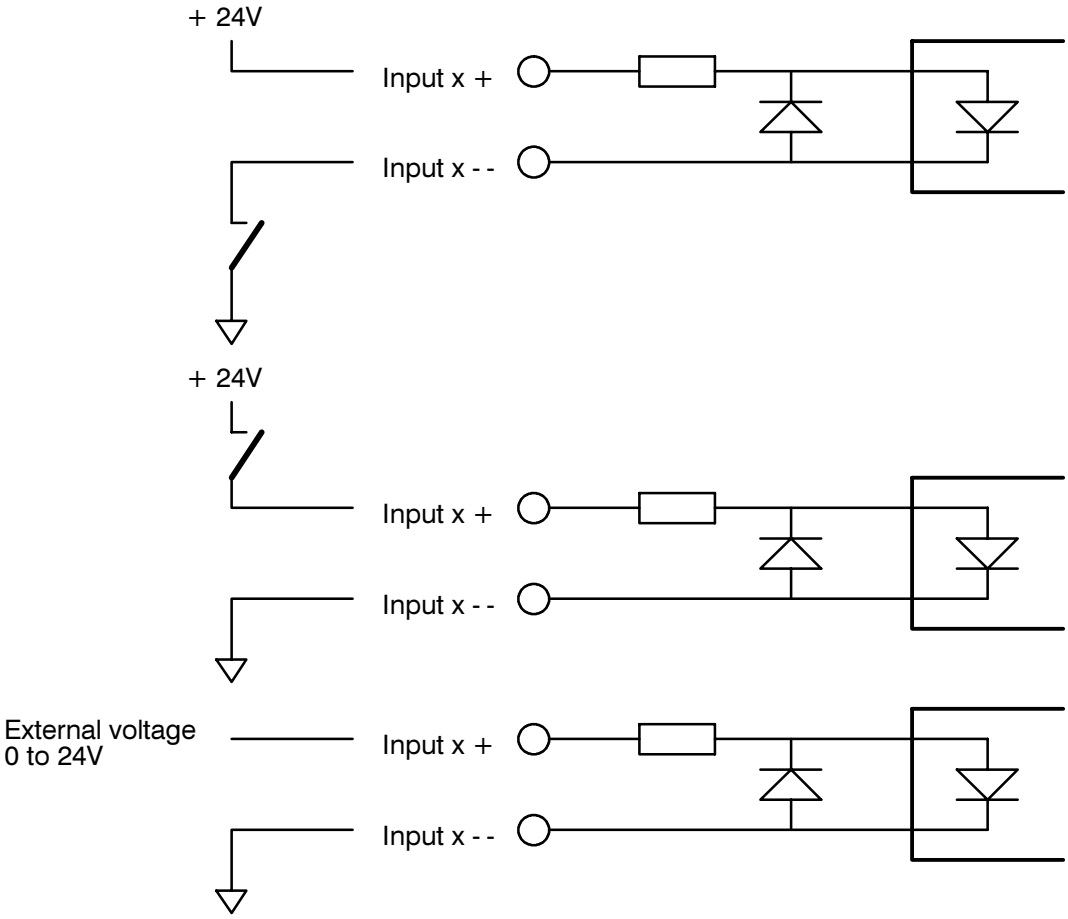


Figure 12: Input Wiring Options

6. IP I/O connector

6.1. Input Connections

Pin-Number	Function	Comment
01	Input 1 +	
02	Input 1 -	
03	Input 2 +	
04	Input 2 -	
05	Input 3 +	
06	Input 3 -	
07	Input 4 +	
08	Input 4 -	
09	Input 5 +	
10	Input 5 -	
11	Input 6 +	
12	Input 6 -	
13	Input 7 +	
14	Input 7 -	
15	Input 8 +	
16	Input 8 -	
17	Input 9 +	
18	Input 9 -	
19	Input 10 +	
20	Input 10 -	
21	Input 11 +	
22	Input 11 -	
23	Input 12 +	
24	Input 12 -	
25	Input 13 +	
26	Input 13 -	
27	Input 14 +	
28	Input 14 -	
29	Input 15 +	
30	Input 15 -	
31	Input 16 +	
32	Input 16 -	

Figure 13: TIP605 Input I/O Connection