# TIP866

8 Channel Serial Interface IP

Version 1.0 Revision B

# User Manual

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**D75866802**

TEWS DATEN*TECHNIK* GmbH
Am Bahnhof 7
D-25469 Halstenbek
Germany
Tel +49 (0)4101 4058-0
Fax +49 (0)4101 4058-19

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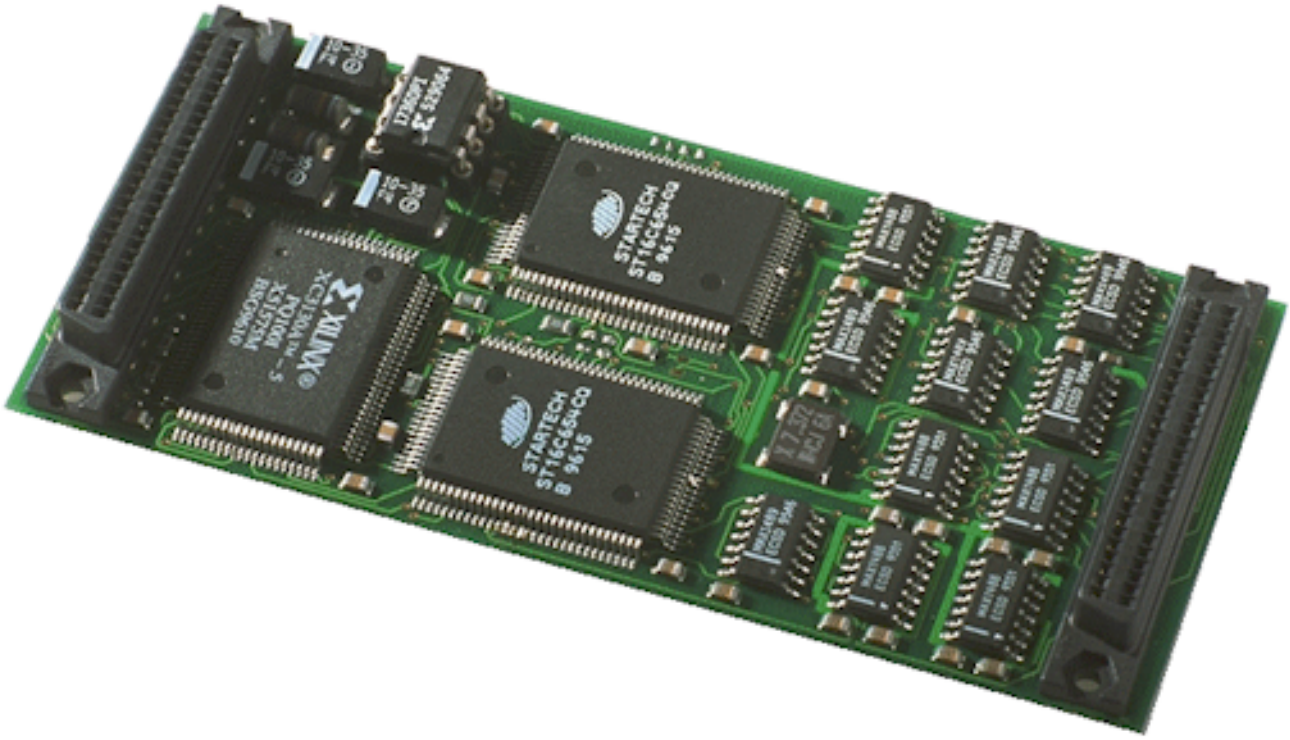

# TIP866-10
## 8 channel RS232 serial I/O

# TIP866-11
## 8 channel TTL serial I/O

# TIP866-20
## 8 channel RS422 serial I/O

This manual covers all products



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# 1. Product Description

The TIP866 provides eight channels of a high performance serial interface. Three different versions are available. The TIP866-10 provides 8 channel RS232 interface, TIP866-11 provides 8 channel TTL interface and the TIP866-20 provides 8 channel RS422 Interface.

Full modem control is available for 2 of the 8 serial interfaces on each TIP866-10/11 (RS232 and TTL Interface only). The TIP866-10/11 supports Receive Data (RxD), Transmit Data (TxD), Ready-To-Send (RTS), Clear-To-Send (CTS) and GND for each channel. Additionally channel one and channel two support Data-Set-Ready (DSR), Data-Terminal-Ready (DTR), Data-Carrier-Detect (DCD) and Ring-detect-Indicator (RI).

The TIP866-20 provides RS422 signal levels by differential transmitters and receivers. Differential transmit data ( TxD +/- ) and receive data ( RxD +/- ) lines are provided, plus ground. The RS422 is preferred over RS232 because it provides significantly higher noise immunity and no ±12V power is required at either the receive or send end. The Receiver Signal termination is 120Ω between RxD+ and RxD-.

Each of the eight serial channels of the TIP866-xx has a 64 byte transmit FIFO and an 64 byte receive FIFO to significantly reduce the overhead required to provide data to and get data from the transmitters and receivers. FIFO trigger level are programmable.

Baud rate is individually programmable up to 115.2 Kbaud for each of the eight RS232 interfaces of the TIP866-10 and up to 460.8 Kbaud for each of the eight TTL/RS422 interfaces of the TIP866-11 or TIP866-20.

Vectored interrupts are provided. Channels 1-4 generate interrupts on interrupt request line $\overline{\text{IP\_INTREQ0}}$ and channel 5-8 generate interrupts on interrupt request line $\overline{\text{IP\_INTREQ1}}$.

Each RS232/RS422 receiver input and transmitter output is protected against electrostatic discharge (ESD). For TIP866-10 (RS232) only diodes places in series with ±12V supply leads will protect the line drivers in the fault condition of connecting powered equipment, even if the TIP866-10 is unpowered.

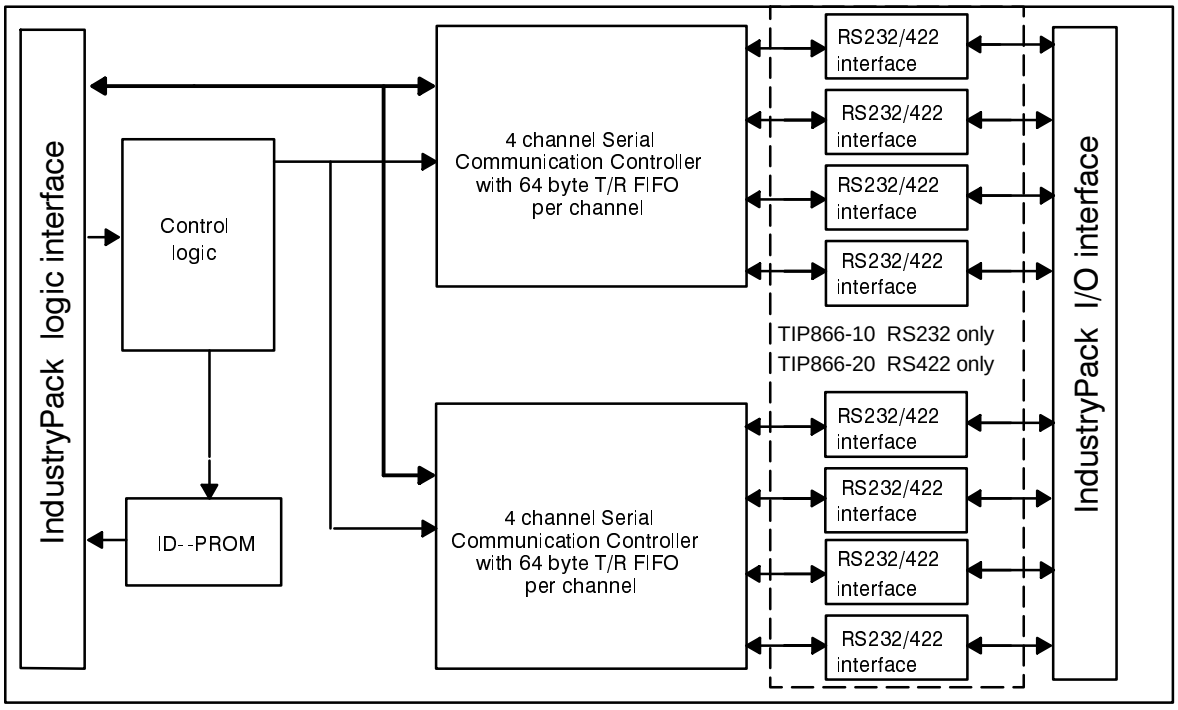


Figure 1: TIP866 Block Diagram

# 2. Technical Specification

| | | |
|---|---|---|
| Logic Interface | IndustryPack® Logic Interface | |
| I/O Interface | 50-conductor flat cable | |
| Size | single wide IP | |
| Number of Channels | Eight | |
| I/O Signals | TIP866-10 (RS232) and TIP866-11 (TTL)<br>TxD, RTS, RxD, CTS, GND<br>DTR, DSR, DCD, RI additionally for channel 1 and channel 2<br><br>TIP866-20 (RS422)<br>TxD+, TxD-, RxD+, RxD-, GND | |
| Termination | 120Ω between RxD+ and RxD- of TIP866-20 | |
| ESD Protection | RS232/422 Transmitter | ±6kV IEC1000-4-2, Contact Discarge<br>±15kV IEC1000-4-2, Air-Gap Discarge |
| | RS232/422 Receiver | ±8kV IEC1000-4-2, Contact Discarge<br>±15kV IEC1000-4-2, Air-Gap Discarge |
| Serial Controller | 2 * ST16C654 ( Quad UART ) | |
| FIFO | 64 byte transmit FIFO, 64 byte receive FIFO per channel | |
| Baud Rates | each channel individually programmable up to 115.2 Kbaud for RS232 Interface and up to 460.8 Kbaud for RS422 and TTL Interface. | |
| Interrupts | Vectored interrupts | $\overline{\text{IP\_INTREQ0}}$ for channel 1-4<br>$\overline{\text{IP\_INTREQ1}}$ for channel 5-8 |
| Wait States | no wait states | |
| Power Requirements | 40mA @ +5V typical ( no serial channels connected)<br>1mA @ -12V typical ( no serial channels connected )<br>1mA @ +12V typical ( no serial channels connected ) | |
| Temperature Range | Operating 0°C to 70°C<br>Storage -40°C to 125°C | |
| Humidity | 5 - 95% non-condensing | |

# 3. ID Prom Contents

## 3.1. ID PROM Contents TIP866-xx V1.0

| ADDRESS | FUNCTION | |
|---|---|---|
| $ 01 | ASCII 'I' | $ 49 |
| $ 03 | ASCII 'P' | $ 50 |
| $ 05 | ASCII 'A' | $ 41 |
| $ 07 | ASCII 'C' | $ 43 |
| $ 09 | Manufacturer ID | $ B3 |
| $ 0B | Model Number | $ 1D |
| $ 0D | Revision | $ 10 |
| $ 0F | RESERVED | $ 00 |
| $ 11 | Driver-ID low-byte | $ 00 |
| $ 13 | Driver-ID high-byte | $ 00 |
| $ 15 | number of bytes | $ 0D |
| $ 17 | C R C | $ see Table 2 |
| $ 19 | Version-xx | $ see Table 2 |
| $ 1B | | $ 00 |
| ..... | not used | ..... |
| $3F | | $ 00 |

Table 1: ID PROM Contents

## 3.2. ID PROM Contents TIP866 Model Depen` dent

| TIP866 | CRC $17 | Version $19 |
|---|---|---|
| - 10 | $ 07 | $ 0A |
| - 11 | $ 26 | $ 0B |
| - 20 | $ F8 | $ 14 |

Table 2: ID PROM Contents Model Dependent

# 4. IP Addressing

All registers of the eight serial channels and the three special registers of the TIP866 are accessible in the I/O space:

| | |
|---|---|
| Channel 1 | IP_I/O_base_address + ($00 to $0F) |
| Channel 2 | IP_I/O_base_address + ($10 to $1F) |
| Channel 3 | IP_I/O_base_address + ($20 to $2F) |
| Channel 4 | IP_I/O_base_address + ($30 to $3F) |
| Channel 5 | IP_I/O_base_address + ($40 to $4F) |
| Channel 6 | IP_I/O_base_address + ($50 to $5F) |
| Channel 7 | IP_I/O_base_address + ($60 to $6F) |
| Channel 8 | IP_I/O_base_address + ($70 to $7F) |
| | |
| INTVEC | IP_I/O_base_address + $0F |
| FIFORDY1 | IP_I/O_base_address + $1F |
| FIFORDY2 | IP_I/O_base_address + $5F |

Table 3: TIP866 I/O Address Map

The three special registers INTVEC, FIFORDY1 and FIFORDY2 of the TIP866 are located inside the register sets of serial channel 1, 2 and 6.

For more details on the ST16C654, its internal registers and its programming see the ST16C654 Data Sheet, which is part of the TIP866-EK engineering kit.

## 4.1. TIP866 Register Map

The TIP866 is accessed in the I/O space through the following registers of the two ST16C654 Quad Universal Asynchronous Receiver/Transmitter (QUART)
Each of the eight serial channels consists of two register sets. Both register sets have a common register, the Line Control Register. Bit 7 of the Line Control Register is used to switch between the register sets of a channel.

### 4.1.1. Register Set Channel 1

Register Set 1 is accessible only if Bit7 of the Line Control Register (LCR, address $07) is set to '0'. After RESET Register Set 1 is accessible.
The special register INTVEC of the TIP866 is accessible within this register set.

| IP-I/O-Base+ | READ MODE | WRITE MODE | SIZE |
|---|---|---|---|
| $ 01 | Receive Holding Reg. | Transmit Holding Reg. | byte |
| $ 03 | Interrupt Enable Reg. | Interrupt Enable Reg. | byte |
| $ 05 | Interrupt Status Reg. | FIFO Control Reg. | byte |
| $ 07 | Line Control Reg. | Line Control Reg. | byte |
| $ 09 | Modem Control Reg. | Modem Control Reg. | byte |
| $ 0B | Line Status Reg. | - | byte |
| $ 0D | Modem Status Reg. | - | byte |
| $ 0F | Interrupt Vector | Interrupt Vector | byte |

Table 4: Register Set 1 Channel 1

To get access to Register Set 2 of channel 1 bit 7 of the Line Control Register (LCR, address $07) must be set to '1'. The Enhance Feature Register, Xon-1,-2 and Xoff-1,-2 registers are accessible only when LCR is set to '$BF'.

| IP-I/O-Base+ | READ/WRITE | SIZE | Comment |
|---|---|---|---|
| $ 01 | LSB of Divisor Latch | byte | LCR bit-7 set to '1' |
| $ 03 | MSB of Divisor Latch | byte | LCR bit-7 set to '1' |
| $ 05 | Enhanced Feature Reg. | byte | LCR is set to '$ BF' |
| $ 07 | Line Control Register (LCR) | byte | always accessible |
| $ 09 | Xon-1 Word | byte | LCR is set to '$ BF |
| $ 0B | Xon-2 Word | byte | LCR is set to '$ BF' |
| $ 0D | Xoff-1 Word | byte | LCR is set to '$ BF' |
| $ 0F | Xoff-2 Word | byte | LCR is set to '$ BF' |

Table 5: Register Set 2 Channel 1

### 4.1.2. Register Set Channel 2

Register Set 1 is accessible only if Bit7 of the Line Control Register (LCR, address $17) is set to '0'. After RESET Register Set 1 is accessible.
The special register FIFORDY1 of the TIP866 is accessible within this register set.

| IP-I/O-Base+ | READ MODE | WRITE MODE | SIZE |
|---|---|---|---|
| $ 11 | Receive Holding Reg. | Transmit Holding Reg. | byte |
| $ 13 | Interrupt Enable Reg. | Interrupt Enable Reg. | byte |
| $ 15 | Interrupt Status Reg. | FIFO Control Reg. | byte |
| $ 17 | Line Control Reg. | Line Control Reg. | byte |
| $ 19 | Modem Control Reg. | Modem Control Reg. | byte |
| $ 1B | Line Status Reg. | - | byte |
| $ 1D | Modem Status Reg. | - | byte |
| $ 1F | FIFORDY1 Reg. | FIFORDY1 Reg. | byte |

Table 6: Register Set 1 Channel 2

To get access to Register Set 2 of channel 2 bit 7 of the Line Control Register (LCR, address $017) must be set to '1'. The Enhance Feature Register, Xon-1,-2 and Xoff-1,-2 registers are accessible only when LCR is set to '$BF'.

| IP-I/O-Base+ | READ/WRITE | SIZE | Comment |
|---|---|---|---|
| $ 11 | LSB of Divisor Latch | byte | LCR bit-7 set to '1' |
| $ 13 | MSB of Divisor Latch | byte | LCR bit-7 set to '1' |
| $ 15 | Enhanced Feature Reg. | byte | LCR is set to '$ BF' |
| $ 17 | Line Control Register (LCR) | byte | always accessible |
| $ 19 | Xon-1 Word | byte | LCR is set to '$ BF |
| $ 1B | Xon-2 Word | byte | LCR is set to '$ BF' |
| $ 1D | Xoff-1 Word | byte | LCR is set to '$ BF' |
| $ 1F | Xoff-2 Word | byte | LCR is set to '$ BF' |

Table 7: Register Set 2 Channel 2

### 4.1.3. Register Set Channel 3

Register Set 1 is accessible only if Bit7 of the Line Control Register (LCR, address $27) is set to '0'. After RESET Register Set 1 is accessible.

| IP-I/O-Base+ | READ MODE | WRITE MODE | SIZE |
|---|---|---|---|
| $ 21 | Receive Holding Reg. | Transmit Holding Reg. | byte |
| $ 23 | Interrupt Enable Reg. | Interrupt Enable Reg. | byte |
| $ 25 | Interrupt Status Reg. | FIFO Control Reg. | byte |
| $ 27 | Line Control Reg. | Line Control Reg. | byte |
| $ 29 | Modem Control Reg. | Modem Control Reg. | byte |
| $ 2B | Line Status Reg. | - | byte |
| $ 2D | Modem Status Reg. | - | byte |
| $ 2F | not used | not used | byte |

Table 8: Register Set 1 Channel 3

To get access to Register Set 2 of channel 3 bit 7 of the Line Control Register (LCR, address $27) must be set to '1'. The Enhance Feature Register, Xon-1,-2 and Xoff-1,-2 registers are accessible only when LCR is set to '$BF'.

| IP-I/O-Base+ | READ/WRITE | SIZE | Comment |
|---|---|---|---|
| $ 21 | LSB of Divisor Latch | byte | LCR bit-7 set to '1' |
| $ 23 | MSB of Divisor Latch | byte | LCR bit-7 set to '1' |
| $ 25 | Enhanced Feature Reg. | byte | LCR is set to '$ BF' |
| $ 27 | Line Control Register (LCR) | byte | always accessible |
| $ 29 | Xon-1 Word | byte | LCR is set to '$ BF |
| $ 2B | Xon-2 Word | byte | LCR is set to '$ BF' |
| $ 2D | Xoff-1 Word | byte | LCR is set to '$ BF' |
| $ 2F | Xoff-2 Word | byte | LCR is set to '$ BF' |

Table 9: Register Set 2 Channel 3

### 4.1.4. Register Set Channel 4

Register Set 1 is accessible only if Bit7 of the Line Control Register (LCR, address $37) is set to '0'. After RESET Register Set 1 is accessible.

| IP-I/O-Base+ | READ MODE | WRITE MODE | SIZE |
|---|---|---|---|
| $ 31 | Receive Holding Reg. | Transmit Holding Reg. | byte |
| $ 33 | Interrupt Enable Reg. | Interrupt Enable Reg. | byte |
| $ 35 | Interrupt Status Reg. | FIFO Control Reg. | byte |
| $ 37 | Line Control Reg. | Line Control Reg. | byte |
| $ 39 | Modem Control Reg. | Modem Control Reg. | byte |
| $ 3B | Line Status Reg. | - | byte |
| $ 3D | Modem Status Reg. | - | byte |
| $ 3F | not used | not used | byte |

Table 10: Register Set 1 Channel 4

To get access to Register Set 2 of channel 4 bit 7 of the Line Control Register (LCR, address $37) must be set to '1'. The Enhance Feature Register, Xon-1,-2 and Xoff-1,-2 registers are accessible only when LCR is set to '$BF'.

| IP-I/O-Base+ | READ/WRITE | SIZE | Comment |
|---|---|---|---|
| $ 31 | LSB of Divisor Latch | byte | LCR bit-7 set to '1' |
| $ 33 | MSB of Divisor Latch | byte | LCR bit-7 set to '1' |
| $ 35 | Enhanced Feature Reg. | byte | LCR is set to '$ BF' |
| $ 37 | Line Control Register (LCR) | byte | always accessible |
| $ 39 | Xon-1 Word | byte | LCR is set to '$ BF |
| $ 3B | Xon-2 Word | byte | LCR is set to '$ BF' |
| $ 3D | Xoff-1 Word | byte | LCR is set to '$ BF' |
| $ 3F | Xoff-2 Word | byte | LCR is set to '$ BF' |

Table 11: Register Set 2 Channel 4

### 4.1.5. Register Set Channel 5

Register Set 1 is accessible only if Bit7 of the Line Control Register (LCR, address $47) is set to '0'. After RESET Register Set 1 is accessible.

| IP-I/O-Base+ | READ MODE | WRITE MODE | SIZE |
|---|---|---|---|
| $ 41 | Receive Holding Reg. | Transmit Holding Reg. | byte |
| $ 43 | Interrupt Enable Reg. | Interrupt Enable Reg. | byte |
| $ 45 | Interrupt Status Reg. | FIFO Control Reg. | byte |
| $ 47 | Line Control Reg. | Line Control Reg. | byte |
| $ 49 | Modem Control Reg. | Modem Control Reg. | byte |
| $ 4B | Line Status Reg. | - | byte |
| $ 4D | Modem Status Reg. | - | byte |
| $ 4F | not used | not used | byte |

Table 12: Register Set 1 Channel 5

To get access to Register Set 2 of channel 5 bit 7 of the Line Control Register (LCR, address $47) must be set to '1'. The Enhance Feature Register, Xon-1,-2 and Xoff-1,-2 registers are accessible only when LCR is set to '$BF'.

| IP-I/O-Base+ | READ/WRITE | SIZE | Comment |
|---|---|---|---|
| $ 41 | LSB of Divisor Latch | byte | LCR bit-7 set to '1' |
| $ 43 | MSB of Divisor Latch | byte | LCR bit-7 set to '1' |
| $ 45 | Enhanced Feature Reg. | byte | LCR is set to '$ BF' |
| $ 47 | Line Control Register (LCR) | byte | always accessible |
| $ 49 | Xon-1 Word | byte | LCR is set to '$ BF |
| $ 4B | Xon-2 Word | byte | LCR is set to '$ BF' |
| $ 4D | Xoff-1 Word | byte | LCR is set to '$ BF' |
| $ 4F | Xoff-2 Word | byte | LCR is set to '$ BF' |

Table 13: Register Set 2 Channel 5

### 4.1.6. Register Set Channel 6

Register Set 1 is accessible only if Bit7 of the Line Control Register (LCR, address $57) is set to '0'. After RESET Register Set 1 is accessible.
The special register FIFORDY2 of the TIP866 is accessible within this register set.

| IP-I/O-Base+ | READ MODE | WRITE MODE | SIZE |
|---|---|---|---|
| $ 51 | Receive Holding Reg. | Transmit Holding Reg. | byte |
| $ 53 | Interrupt Enable Reg. | Interrupt Enable Reg. | byte |
| $ 55 | Interrupt Status Reg. | FIFO Control Reg. | byte |
| $ 57 | Line Control Reg. | Line Control Reg. | byte |
| $ 59 | Modem Control Reg. | Modem Control Reg. | byte |
| $ 5B | Line Status Reg. | - | byte |
| $ 5D | Modem Status Reg. | - | byte |
| $ 5F | FIFORDY2 Reg. | FIFORDY2 Reg. | byte |

Table 14: Register Set 1 Channel 6

To get access to Register Set 2 of channel 6 bit 7 of the Line Control Register (LCR, address $57) must be set to '1'. The Enhance Feature Register, Xon-1,-2 and Xoff-1,-2 registers are accessible only when LCR is set to '$BF'.

| IP-I/O-Base+ | READ/WRITE | SIZE | Comment |
|---|---|---|---|
| $ 51 | LSB of Divisor Latch | byte | LCR bit-7 set to '1' |
| $ 53 | MSB of Divisor Latch | byte | LCR bit-7 set to '1' |
| $ 55 | Enhanced Feature Reg. | byte | LCR is set to '$ BF' |
| $ 57 | Line Control Register (LCR) | byte | always accessible |
| $ 59 | Xon-1 Word | byte | LCR is set to '$ BF |
| $ 5B | Xon-2 Word | byte | LCR is set to '$ BF' |
| $ 5D | Xoff-1 Word | byte | LCR is set to '$ BF' |
| $ 5F | Xoff-2 Word | byte | LCR is set to '$ BF' |

Table 15: Register Set 2 Channel 6

### 4.1.7. Register Set Channel 7

Register Set 1 is accessible only if Bit7 of the Line Control Register (LCR, address $67) is set to '0'. After RESET Register Set 1 is accessible.

| IP-I/O-Base+ | READ MODE | WRITE MODE | SIZE |
|---|---|---|---|
| $ 61 | Receive Holding Reg. | Transmit Holding Reg. | byte |
| $ 63 | Interrupt Enable Reg. | Interrupt Enable Reg. | byte |
| $ 65 | Interrupt Status Reg. | FIFO Control Reg. | byte |
| $ 67 | Line Control Reg. | Line Control Reg. | byte |
| $ 69 | Modem Control Reg. | Modem Control Reg. | byte |
| $ 6B | Line Status Reg. | - | byte |
| $ 6D | Modem Status Reg. | - | byte |
| $ 6F | not used | not used | byte |

Table 16: Register Set 1 Channel 7

To get access to Register Set 2 of channel 7 bit 7 of the Line Control Register (LCR, address $67) must be set to '1'. The Enhance Feature Register, Xon-1,-2 and Xoff-1,-2 registers are accessible only when LCR is set to '$BF'.

| IP-I/O-Base+ | READ/WRITE | SIZE | Comment |
|---|---|---|---|
| $ 61 | LSB of Divisor Latch | byte | LCR bit-7 set to '1' |
| $ 63 | MSB of Divisor Latch | byte | LCR bit-7 set to '1' |
| $ 65 | Enhanced Feature Reg. | byte | LCR is set to '$ BF' |
| $ 67 | Line Control Register (LCR) | byte | always accessible |
| $ 69 | Xon-1 Word | byte | LCR is set to '$ BF |
| $ 6B | Xon-2 Word | byte | LCR is set to '$ BF' |
| $ 6D | Xoff-1 Word | byte | LCR is set to '$ BF' |
| $ 6F | Xoff-2 Word | byte | LCR is set to '$ BF' |

Table 17: Register Set 2 Channel 7

### 4.1.8. Register Set Channel 8

Register Set 1 is accessible only if Bit7 of the Line Control Register (LCR, address $77) is set to '0'. After RESET Register Set 1 is accessible.

| IP-I/O-Base+ | READ MODE | WRITE MODE | SIZE |
|---|---|---|---|
| $ 71 | Receive Holding Reg. | Transmit Holding Reg. | byte |
| $ 73 | Interrupt Enable Reg. | Interrupt Enable Reg. | byte |
| $ 75 | Interrupt Status Reg. | FIFO Control Reg. | byte |
| $ 77 | Line Control Reg. | Line Control Reg. | byte |
| $ 79 | Modem Control Reg. | Modem Control Reg. | byte |
| $ 7B | Line Status Reg. | - | byte |
| $ 7D | Modem Status Reg. | - | byte |
| $ 7F | not used | not used | byte |

Table 18: Register Set 1 Channel 8

To get access to Register Set 2 of channel 8 bit 7 of the Line Control Register (LCR, address $77) must be set to '1'. The Enhance Feature Register, Xon-1,-2 and Xoff-1,-2 registers are accessible only when LCR is set to '$BF'.

| IP-I/O-Base+ | READ/WRITE | SIZE | Comment |
|---|---|---|---|
| $ 71 | LSB of Divisor Latch | byte | LCR bit-7 set to '1' |
| $ 73 | MSB of Divisor Latch | byte | LCR bit-7 set to '1' |
| $ 75 | Enhanced Feature Reg. | byte | LCR is set to '$ BF' |
| $ 77 | Line Control Register (LCR) | byte | always accessible |
| $ 79 | Xon-1 Word | byte | LCR is set to '$ BF |
| $ 7B | Xon-2 Word | byte | LCR is set to '$ BF' |
| $ 7D | Xoff-1 Word | byte | LCR is set to '$ BF' |
| $ 7F | Xoff-2 Word | byte | LCR is set to '$ BF' |

Table 19: Register Set 2 Channel 8

## 4.2. Special Registers

### 4.2.1. Interrupt Vector Register Address $0F

The Interrupt Vector Register INTVEC is a byte wide read/write register. It is located within the Register Set 1 of channel 1.
The Interrupt Vector Register is shared between both interrupt sources ( controller 1 for channel 1-4 and controller 2 for channel 5-8 ). Each controller generates an individual interrupt.

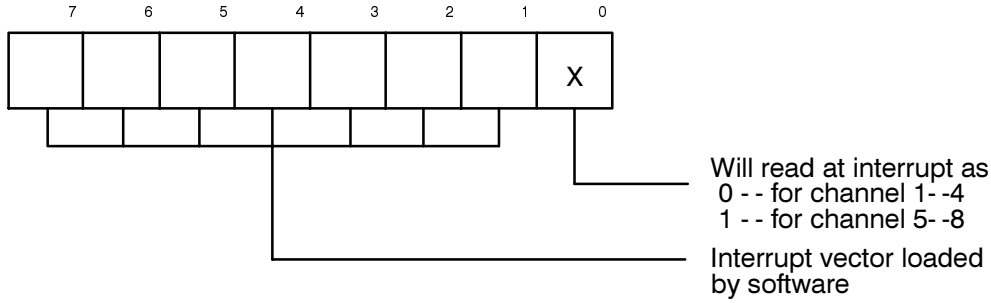


Figure 2: INTVEC Interrupt Vector Register

For an interrupt from controller 1 ( channel 1-4) bit 0 of the interrupt vector will read as '0'. For an interrupt from controller 2 ( channel 5-8) bit 0 will read as '1'. If the Interrupt Vector Register is for example loaded with '$60', controller1 will create an interrupt at vector '$60' and controller 2 will create an interrupt at vector '$61'.
In I/O space D0 of the interrupt vector register always read as '1'.

**Note**

Controller 1 of the TIP866 generate interrupts on interrupt request line $\overline{\text{INTREQ0}}$ and Controller 2 of the TIP866 generate interrupts on interrupt request line $\overline{\text{INTREQ0}}$ of the IP- -bus.

### 4.2.2. FIFO Ready Status Register Channel 1-4 Address $1F

The FIFO Ready Status Register FIFORDY1 is a byte wide read only register. It is located within the Register Set 1 of channel 2.

If a serial channel of controller 1 of the TIP866-xx is in FIFO mode (FIFO Control Register bit 0 set to 1 ) and bit 3 of the FIFO Control Register is set to 1 the corresponding TxRdy-bit of the FIFORDY1 register will be read as 1 when the transmit FIFO is completely full. It will be read as 0 if one or more transmit FIFO locations of the channel are empty.
The corresponding RxRdy-bit of the FIFORDY1 register will become 0 when the FIFO trigger level has been reached. The RxRdy-bit of the FIFORDY1 register will be read as 1 when there are no more characters in the receive FIFO.

If a serial channel of controller 1 of the TIP866-xx is in FIFO mode (FIFO Control Register bit 0 set to 1 ) and bit 3 of the FIFO Control Register is set to 0 or if the FIFO mode is disabled
the TxRdy-bit of the FIFORDY1 register will be read as 0 when there are no characters in the transmit FIFO or transmit holding register. The TxRdy-bit of the FIFORDY1 register will be read as 1 after the first character is loaded into the transmit register.
The corresponding RxRdy-bit of the FIFORDY1 register will be read as 0 when there is at least 1 character in the receive FIFO. The RxRdy-bit of the FIFORDY1 register will be read as 1 when there are no more characters in the receiver.

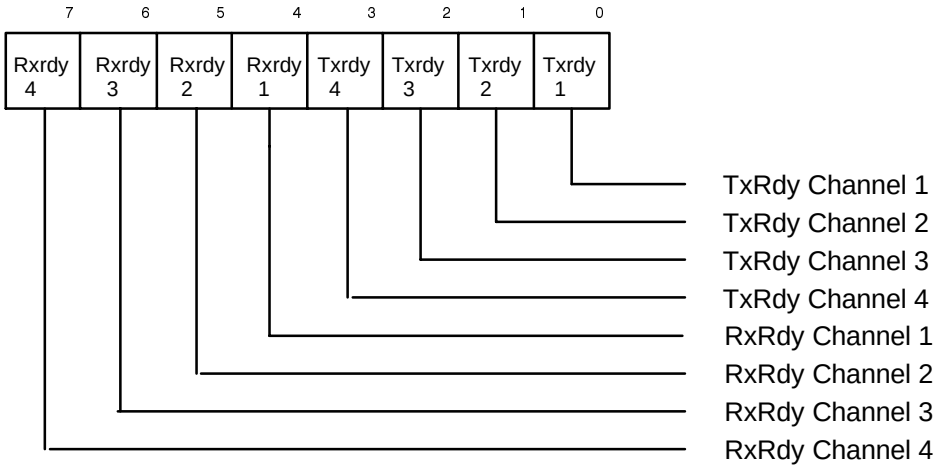


Figure 3: FIFORDY1 Register

**Note**

After RESET the FIFORDY1 register will be read as $F0.

### 4.2.3. FIFO Ready Status Register Channel 5-8 Address $5F

The FIFO Ready Status Register FIFORDY2 is a byte wide read only register. It is located within the Register Set 1 of channel 6.

If a serial channel of controller 2 of the TIP866-xx is in FIFO mode (FIFO Control Register bit 0 set to 1 ) and bit 3 of the FIFO Control Register is set to 1 the corresponding TxRdy-bit of the FIFORDY2 register will be read as 1 when the transmit FIFO is completely full. It will be read as 0 if one or more transmit FIFO locations of the channel are empty.
The corresponding RxRdy-bit of the FIFORDY2 register will become 0 when the FIFO trigger level has been reached. The RxRdy-bit of the FIFORDY1 register will be read as 1 when there are no more characters in the receive FIFO.

If a serial channel of controller 2 of the TIP866-xx is in FIFO mode (FIFO Control Register bit 0 set to 1 ) and bit 3 of the FIFO Control Register is set to 0 or if the FIFO mode is disabled
the TxRdy-bit of the FIFORDY2 register will be read as 0 when there are no characters in the transmit FIFO or transmit holding register. The TxRdy-bit of the FIFORDY2 register will be read as 1 after the first character is loaded into the transmit register.
The corresponding RxRdy-bit of the FIFORDY2 register will be read as 0 when there is at least 1 character in the receive FIFO. The RxRdy-bit of the FIFORDY2 register will be read as 1 when there are no more characters in the receiver.

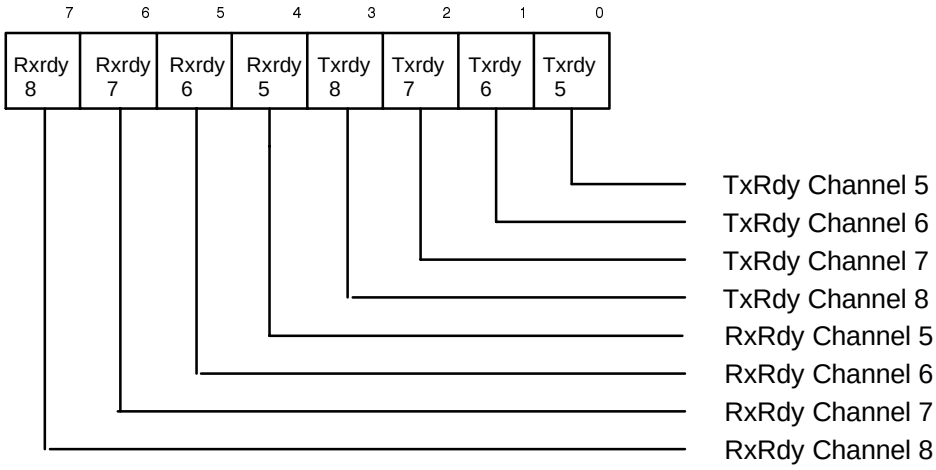


Figure 4: FIFORDY2 Register

**Note**

After RESET the FIFORDY2 register will be read as $F0.

# 5. Baud Rate Programming

Each of the eight serial channels of the TIP866-xx contains a programmable Baud Rate Generator. The clock of the ST16C654 can be divided by any Divisor from 1 to $2^{16}$-1. The Divisor can be programmed by the LSB of Divisor Latch Register and MSB of Divisor Latch Register. After RESET the MCR Bit7 of each serial channel defaults to '1' and the value of LSB and MSB of Divisor Latch is $FFFF.

## 5.1. Baud Rate Programming Formula

The basic formula of baud rate programming is:

Baud Rate = 7.372MHz / (( 16 * DIVISOR ) * ( 1 + 3 * MCR Bit7 ))

| BAUD RATE MCR BIT7=0 | BAUD RATE MCR BIT7=1 | DIVISOR |
|---|---|---|
| 200 | 50 | $0900 |
| 300 | 75 | $0600 |
| 600 | 150 | $0300 |
| 1200 | 300 | $0180 |
| 2400 | 600 | $00C0 |
| 4800 | 1200 | $0060 |
| 9600 | 2400 | $0030 |
| 19.2K | 4800 | $0018 |
| 28.8K | 7200 | $0010 |
| 38.4K | 9600 | $000C |
| 76.8K | 19.2K | $0006 |
| 153.6K | 38.4K | $0003 |
| 230.4K | 57.6K | $0002 |
| 460.8K | 115.2K | $0001 |

Table 20: Baud Rate Programming Table

The highest data rate of the TIP866-10 is 115.2Kbaud because of the RS232 Line Drivers and Receivers. For using higher data rates (230.4K and 460.8K) the MCR Bit7 must be set to '0' (only for TIP866-11/20 with TTL or RS422 Interface).

# 6. I/O Pin Assignment

## 6.1. 50 Pin I/O Connector TIP866-1x RS232/TTL

| Pin--Number | TIP866--10/11 | Comment |
|---|---|---|
| 1 | GND | Signal Ground |
| 2 | TXD1 | active low |
| 3 | RXD1 | active low |
| 4 | RTS1 | active high |
| 5 | CTS1 | active high |
| 6 | GND | Signal Ground |
| 7 | TXD2 | active low |
| 8 | RXD2 | active low |
| 9 | RTS2 | active high |
| 10 | CTS2 | active high |
| 11 | GND | Signal Ground |
| 12 | TXD3 | active low |
| 13 | RXD3 | active low |
| 14 | RTS3 | active high |
| 15 | CTS3 | active high |
| 16 | GND | Signal Ground |
| 17 | TXD4 | active low |
| 18 | RXD4 | active low |
| 19 | RTS4 | active high |
| 20 | CTS4 | active high |
| 21 | GND | Signal Ground |
| 22 | TXD5 | active low |
| 23 | RXD5 | active low |
| 24 | RTS5 | active high |
| 25 | CTS5 | active high |
| 26 | GND | Signal Ground |
| 27 | TXD6 | active low |
| 28 | RXD6 | active low |
| 29 | RTS6 | active high |
| 30 | CTS6 | active high |
| 31 | GND | Signal Ground |
| 32 | TXD7 | active low |
| 33 | RXD7 | active low |
| 34 | RTS7 | active high |
| 35 | CTS7 | active high |
| 36 | GND | Signal Ground |
| 37 | TXD8 | active low |
| 38 | RXD8 | active low |
| 39 | RTS8 | active high |

| Pin--Number | TIP866--10/11 | Comment |
|---|---|---|
| 40 | CTS8 | active high |
| 41 | DCD1 | active high |
| 42 | DTR1 | active high |
| 43 | RI1 | active high |
| 44 | DSR1 | active high |
| 45 | DCD2 | active high |
| 46 | DTR2 | active high |
| 47 | RI2 | active high |
| 48 | DSR2 | active high |
| 49 | +5V | Supply for Transition Module |
| 50 | GND | Supply for Transition Module |

Table 21: I/O Pin Assignment TIP866-10/11

**Note**

For TTL Interface TIP866--11 the signal activity is inverse

## 6.2. 50 Pin I/O Connector TIP866-20 RS422

| Pin--Number | TIP866--20 | Comment/Level |
|---|---|---|
| 1 | GND | Signal Ground |
| 2 | TxD1-- | RS422-- |
| 3 | TxD1+ | RS422+ |
| 4 | RxD1-- | RS422-- |
| 5 | RxD1+ | RS422+ |
| 6 | GND | Signal Ground |
| 7 | TxD2-- | RS422-- |
| 8 | TxD2+ | RS422+ |
| 9 | RxD2-- | RS422-- |
| 10 | RxD2+ | RS422+ |
| 11 | GND | Signal Ground |
| 12 | TxD3-- | RS422-- |
| 13 | TxD3+ | RS422+ |
| 14 | RxD3-- | RS422-- |
| 15 | RxD3+ | RS422+ |
| 16 | GND | Signal Ground |
| 17 | TxD4-- | RS422-- |
| 18 | TxD4+ | RS422+ |
| 19 | RxD4-- | RS422-- |
| 20 | RxD4+ | RS422+ |

| Pin--Number | TIP866--20 | Comment/Level |
|---|---|---|
| 21 | GND | Signal Ground |
| 22 | TxD5-- | RS422-- |
| 23 | TxD5+ | RS422+ |
| 24 | RxD5-- | RS422-- |
| 25 | RxD5+ | RS422+ |
| 26 | GND | Signal Ground |
| 27 | TxD6-- | RS422-- |
| 28 | TxD6+ | RS422+ |
| 29 | RxD6-- | RS422-- |
| 30 | RxD6+ | RS422+ |
| 31 | GND | Signal Ground |
| 32 | TxD7-- | RS422-- |
| 33 | TxD7+ | RS422+ |
| 34 | RxD7-- | RS422-- |
| 35 | RxD7+ | RS422+ |
| 36 | GND | Signal Ground |
| 37 | TxD8-- | RS422-- |
| 38 | TxD8+ | RS422+ |
| 39 | RxD8-- | RS422-- |
| 40 | RxD8+ | RS422+ |
| 41 | GND | Signal Ground |
| 42--50 | N.C. | no connection |

Table 22: I/O Pin Assignment TIP866-20

**Note**

On board signal termination between RxD+ and RxD-- is 120Ω for each channel.